METHOD TO FABRICATE SURFACE P-CHANNEL CMOS

ABSTRACT

An improved method of making CMOS surface channel transistors using fewer masking steps. In-situ doped poly silicon deposition can be used to reduce problems with poly depletion effects in transistor gates. In addition, using this method, the number of layers in each gate dielectric, the dielectric type, and dielectric thickness between n-channel and p-channel devices can be separately controlled. This method also allows the use of a lithography mask normally used to fabricate buried channel devices for use in fabricating surface channel devices, thus saving the manufacture of an additional mask.